Amendments

In the Claims:

Claims 1-5 (Cancelled).

6. (Currently Amended) ~~The memory device according to claim 5~~ A memory device, comprising:

a switch array comprising a plurality of first switches for connecting a lower byte region of a data I/O buffer to a lower byte region of a sense amplifier array, a plurality of second switches for connecting the lower byte region of the data I/O buffer to an upper byte region of the sense amplifier array, and a plurality of third switches for connecting an upper byte region of the data I/O buffer to the upper byte region of the sense amplifier array; and

a switch controller for receiving external control signals to control activation of the data I/O buffer and on/off operations of the first through the third switches,

wherein the switch controller turns on the first switch and activates the lower byte region of the data I/O buffer connected to an I/O port when a lower byte signal included in the external control signal is activated, and turns on the third switch and activates the upper byte region of the data I/O buffer connected to an I/O port when an upper byte signal included in the external control signals ~~signal~~ is activated.

7. (Currently Amended) ~~The memory device according to claim 5~~ A memory device, comprising:

a switch array comprising a plurality of first switches for connecting a lower byte region of a data I/O buffer to a lower byte region of a sense amplifier array, a plurality of second switches for connecting the lower byte region of the data I/O buffer to an upper byte region of the sense amplifier array, and a plurality of third switches for connecting an upper byte region of the data I/O buffer to the upper byte region of the sense amplifier array; and

a switch controller for receiving external control signals to control activation of the data I/O buffer and on/off operations of the first through the third switches,

wherein the lower byte region of the data I/O buffer is connected to an I/O port, the upper byte region of the data I/O buffer is not connected to an I/O port, and an external control signal included in the external signals is provided through a terminal pin connected to the upper byte region of the data I/O buffer.

8. (Original) The memory device according to claim 7, wherein the switch controller activates the first switches when a control signal inputted through the terminal pin is "0", and the second switches when a control signal inputted through the terminal pin is "1".

9. (Currently Amended) The memory device according to claim 6 ~~claim 5~~,

wherein the switch controller inactivates the upper byte region of the data I/O buffer and activates the second switches if a signal inputted through a terminal pin connected to the upper byte region is "1", and activates the first switches if a signal inputted through the terminal pin is "0" when a byte signal included in the external control signals is activated, and

the switch controller turns on the first switches and then activates a lower byte region of the data I/O buffer if a lower byte signal included in the external control signals is activated, and turns on the third switches and then activates an upper region of the data I/O buffer if an upper byte signal included in the external control signal is activated when the byte signal is inactivated.

Claims 10-12 (Cancelled).

13. (Currently Amended) ~~The memory device according to claim 5~~ A memory device, comprising:

a switch array comprising a plurality of first switches for connecting a lower byte region of a data I/O buffer to a lower byte region of a sense amplifier array, a plurality of second switches for connecting the lower byte region of the data I/O buffer to an upper byte region of the sense amplifier array, and a plurality of third switches for connecting an upper byte region of the data I/O buffer to the upper byte region of the sense amplifier array; and

a switch controller for receiving external control signals to control activation of the data I/O buffer and on/off operations of the first through the third switches,

wherein the memory device is a ferroelectric memory device having a bitline structure comprising a main bitline and a plurality of sub bitlines.

Claims 14-17 (Cancelled).

18. (Currently Amended) A memory device that processes data by two bytes comprising a lower byte and an upper byte that is capable of operating with a system that processes data by one byte, comprising:

a plurality of data pads ~~configured to connect~~ connected to the system;

a data input/output buffer coupled to the plurality of data pads and comprising a lower byte ~~portion~~ region and an upper byte ~~portion~~ region;

a circuit that stores data of the lower byte ~~portion~~ region of the data input/output buffer to either an upper byte ~~portion~~ region or a lower byte ~~portion~~ region of data storing portion depending upon an external control signal received on a data pad coupled to the upper byte region ~~portion~~ of the data input/output buffer.

19. (Cancelled).

20. (New) The memory device according to the claim 18, wherein the external control signal is a least significant bit of an address signal.

21. (New) A system comprising the memory device according to the claim 6.

22. (New) A system comprising the memory device according to the claim 7.